REMARKS

Claims 46-48, 51-56, 58-60, 62-65 and 67-74 and 76-91 are pending in this application. Claim 75 has been canceled. Claims 46, 56, 62 and 72-74 have been amended. No new matter has been introduced.

Claims 56, 58-60, 62-65 and 67-71 stand rejected under 35 U.S.C. §112, second paragraph, as being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." (Office Action at 2). Specifically, the Office Action asserts that there is insufficient antecedent basis for the limitation "buried conductor pattern" of claim 56, and for the limitation "conductive structure" of claim 62, at line 11. (Office Action at 2). Claim 56 has been amended to obviate the rejection. Applicants note that the antecedent basis for the limitation "conductive structure" at line 11 of claim 62 appears at line 5 of this claim. Applicants submit that all pending claims are in compliance with 35 U.S.C. §112.

Claims 46, 51, 52, 55, 56, 58, 59 and 72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (U.S. Patent No. 5,963,838) ("Yamamoto") in view of Bai et al. (U.S. Patent No. 5,861,340) ("Bai"). This rejection is respectfully traversed.

The claimed invention relates to semiconductor devices and, in particular, to buried conductors within a substrate. As such, amended independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Amended independent claim 46 also recites that the buried conductor pattern "is completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline

substrate." Amended independent claim 46 further recites "a conductive path extending from said buried conductor pattern to said devices."

Amended independent claim 56 recites a buried conductor pattern within a "monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein." Amended independent claim 56 also recites "a conductive material filling said empty space pattern such that said conductive material is below a top surface of said monocrystalline substrate and forms a buried conductor pattern, said buried conductor pattern being completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate." Amended independent claim 56 further recites "a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate."

Amended independent claim 72 recites an "integrated circuit substrate comprising a plurality of buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate." Amended independent claim 72 also recites that the buried conductor patterns form "at least a part of an interconnect between devices."

Yamamoto relates to a "transistor element . . . formed on the surface of a silicon substrate." (Abstract). According to Yamamoto, "[a] tunnel is formed in the silicon substrate at a position right under the transistor element" and "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). Yamamoto also teaches that "[s]ilicon oxide films are respectively formed

on the inner surfaces of the tunnel and the contact hole" and that "[a] wiring layer is buried in the tunnel and the contact hole." (Abstract).

Bai relates to a "method of forming a polycide thin film." (Abstract). Bai teaches that "[F]irst, a silicon layer is formed" and that "[N]ext, a thin barrier layer is formed on the first silicon layer." (Abstract). According to Bai, "[A] second silicon layer is then formed on the barrier layer" and "a metal layer is formed on the second silicon layer." (Abstract). In this manner, "[T]he metal layer and the second silicon layer are then reacted together to form a silicide." (Abstract).

The subject matter of claims 46, 51, 52, 55, 56, 58, 59 and 72 would not have been obvious over Yamamoto in view of Bai, whether considered alone or in combination. Specifically, the June 13, 2005 Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, neither Yamamoto nor Bai discloses, teaches or suggests all limitations of independent claims 46, 56 and 72. Yamamoto does not teach or suggest a "buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as amended independent claim 46 recites. Yamamoto teaches tunnel 30 which is "formed in the silicon substrate at a position right under the transistor

element" and adjacent n-type well region 25, and not a "buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material *of a same conductivity type* of said monocrystalline substrate," as in the claimed invention (emphasis added).

Further, Yamamoto does not disclose, teach or suggest a "buried conductor pattern . . . being completely surrounded by monocrystalline material," as independent claims 46 and 56 recite. In Yamamoto, wiring layer 32, which would arguably correspond to the "buried conductor pattern" of the claimed invention, is surrounded by substrate 21, well 25 and conductive film 37, and is not "completely surrounded by monocrystalline material," as in the claimed invention.

Yamamoto also does not teach or suggest all limitations of amended independent claim 72. Yamamoto is silent about "a plurality of buried conductor patterns," much less "a plurality of buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and . . . completely surrounded by the same monocrystalline substrate material of said monocrystalline substrate," as amended independent claim 72 recites.

Similarly, Bai is silent about a buried conductor pattern, much less about a "buried conductor pattern" "forming at least a part of an interconnect between devices," much less about a "buried conductor pattern . . . being completely surrounded by monocrystalline material," as in the claimed invention (emphasis added).

Applicants further note that, to establish a *prima facie* case of obviousness, "[i]t is insufficient that the prior art disclosed the components of the patented device,

either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573. This way, a rejection of a claim for obviousness in view of a combination of prior art references must be based on a showing of a suggestion, teaching, or motivation that has to be "clear and particular." In re Dembiczak, 175 F.3d at 999. Thus, the mere fact that it is possible to find two isolated disclosures which might be combined to produce a new compound does not necessarily render such production obvious, unless the prior art also suggests the desirability of the proposed combination.

The June 13, 2005 Office Action fails to establish a *prima facie* case of obviousness because, as the Court in Northern Telecom, Inc. noted, "[i]t is insufficient that the prior art disclosed the components of the patented device" and there is no "teaching, suggestion, or incentive to make the combination." Northern Telecom, Inc., 908 F.2d at 934. On one hand, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). For this, Yamamoto teaches that "[a] tunnel is formed in the silicon substrate at a position right under the transistor element" and that "[a] contact hole is formed to extend from the surface of the silicon substrate to the contact hole." (Abstract). On the other hand, the crux of Bai is a method of forming a polycide film with increased thermal stability. For this, Bai teaches that a plurality of layers are

formed over a substrate as part of a gate electrode and subjected to various thermal conditions. Thus, Yamamoto and Bai do not even have in common the substrate on which their respective structures are formed. In addition, a person of ordinary skill in the art would not have been motivated to combine Yamamoto, which teaches the formation of wiring layers *below* a surface of a substrate, with Bai, which teaches the formation of a thin silicide layer *over* a surface of a substrate.

For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 46, 51, 52, 55, 56, 58, 59 and 72 is respectfully requested.

Claims 47, 48, 76-79 and 81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Bai and further in view of Kenney (U.S. Patent No. 5,583,368). This rejection is respectfully traversed.

Independent claim 76 recites an "integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that said buried conductor patterns are below a top surface of said substrate and said buried conductor patterns are completely surrounded by the same monocrystalline material of said monocystalline substrate." Independent claim 76 also recites that the first and second buried conductive patterns form "at least a part of first and second interconnects between devices, respectively, wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate."

Kenney relates to "[c]hips having subsurface structures within or adjacent a horizontal trench in bulk single crystal semiconductor." (Abstract). According to Kenney, "[s]tructures include three terminal devices, such as FETs and bipolar

transistors, rectifying contacts, such as pn diodes and Schottky diodes, capacitors, and contacts to and connectors between devices." (Abstract). Kenney also teaches a "process for forming a horizontal trench exclusively in heavily doped p+ regions is presented in which porous silicon is first formed in the p+ regions and then the porous silicon is etched." (Abstract).

The subject matter of claims 47, 48, 76-79 and 81 would not have been obvious over Yamamoto, Bai and Kenney. The cited references, considered alone or in combination, fail to disclose, teach or suggest all limitations of independent claims 46 and 76. None of Yamamoto, Bai and Kenney teaches or suggests a "buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as independent claim 46 recites. Moreover, none of the cited references teaches or suggests "first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductors pattern is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate," as independent claim 76 recites. For at least these reasons, the subject matter of claims 47, 48, 76-79 and 81 would not have been obvious over Yamamoto, Bai and Kenney, and withdrawal of the rejection of these claims is respectfully requested.

Claims 53 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Bai and further in view of Witek et al. (U.S. Patent No. 5,291,438) ("Witek"). Claim 54 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Bai and further in view of Noguchi et al. (U.S. Patent No. 6,437,403) ("Noguchi"). These rejections are respectfully traversed.

Claims 53 and 54 depend on amended independent claim 46. As noted above, Yamamoto and Bai, considered alone or in combination, fail to disclose, teach or suggest all limitations of amended independent claim 46. In addition, a person of ordinary skill in the art would not have been motivated to combine Yamamoto and Bai to achieve the claimed invention. Witek and Noguchi fail to supplement the deficiencies of Yamamoto and Bai. For at least these reasons, withdrawal of the rejection of claims 53 and 54 is also respectfully requested.

Claim 60 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Bai and further in view of Sato et al., *A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) Induced by Silicon Surface Migration*, 1999 IEEE, pp. 517-20 ("Sato"). This rejection is respectfully traversed.

Sato relates to a technique for forming empty spaces with various shapes in silicon substrates. Sato emphasizes that "[w]hen deeply-etched silicon substrates are annealed in a deoxidizing ambient, such as a hydrogen ambient, the silicon atoms on the surface migrate so as to minimize the surface energy." (Sato at 517). This way, for example, "trenches arranged in a row are transformed to an empty space shaped like a pipe, due to the combination of the grown empty spheres at the bottom of each trench." (Sato at 517).

The subject matter of claim 60 (which depends on amended independent claim 56) would not have been obvious over Yamamoto in view of Sato, considered alone or in combination. First, Yamamoto and Sato, considered alone or in combination, fail to teach or suggest "a buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as amended independent claim 56 recites.

Yamamoto fails to teach or suggest a buried conductor pattern within a monocrystalline substrate, much less a "buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as in the claimed invention. Sato is also silent about a buried conductor pattern within a monocrystalline substrate, or about a "buried conductor pattern" "forming at least a part of an interconnect between devices," or about a "buried conductor pattern . . . completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate," as in the claimed invention.

Further, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Sato. As noted above, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). Yamamoto teaches "implanting an impurity in a semiconductor substrate . . . to form an impurity-implanted layer in the semiconductor substrate, forming a contact hole extending from a surface of the semiconductor substrate and reaching the impurity-implanted layer, selectively etching the impurity-implanted layer to form a tunnel in the semiconductor substrate, and burying a conductive film in the tunnel and the contact hole." (Col. 6, lines 53-62). According to one embodiment of Yamamoto illustrated in Figures 32-38, "an oxygen-implanted layer 2 is formed in the silicon substrate 1 at a predetermined depth." (Col. 16, lines 49-50; Figure 32). At the time a field oxide film 3 is formed on the silicon substrate 1, "in the oxygen-implanted layer 2 . . . oxygen (O) is combined with silicon (Si) to form an SiO_2 layer 4." (Col. 16, lines 51-54; Figure 33). In contrast, Sato relates to empty space formation in a silicon substrate by drilling holes in the silicon substrate at a predefined depth, and then annealing the substrate at about 1100ºC to form various empty space patterns. It is clear, therefore, that the only

element which Yamamoto and Sato have in common is the silicon substrate in which their respective structures are formed. Accordingly, there is no motivation for a person of ordinary skill in the art to employ the Sato empty-space formation technique in the Yamamoto's method of forming an oxygen implanted layer and subsequently removing such layer.

Applicants also note that the Office Action's proposed combination of Yamamoto with Sato would require a complete reconstruction and redesign of Yamamoto. Courts have held that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 2143.01 (citing In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959). This is because the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which [the primary reference] construction was designed to operate." In re Ratti, 270 F.2d at 813, 123 U.S.P.Q. at 352.

In the present case, employing the empty space technique of Sato *in lieu* of the impurity implanting technique of Yamamoto, as the Office Action suggests, "would require a substantial *reconstruction* and *redesign* of the elements shown in [Yamamoto] (emphasis added)." Thus, the suggested combination of Sato and Yamamoto would have to eliminate the oxygen-implanted layer and the subsequently converted silicon dioxide layer of Yamamoto and, thus, redesign and reconstruct the elements of Yamamoto. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claim 60 is respectfully requested.

Claims 62-64 and 67-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Bai and further in view of Tsu et al. (U.S. Patent No. 6,294,420 B1) ("Tsu"). This rejection is respectfully traversed.

Amended independent claim 62 recites "a processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein." Amended independent claim 62 also recites "a conductive material filling said empty space pattern such that said conductive material is below a top surface of said monocrystalline substrate and said conductive structure is completely surrounded by the same monocrystalline substrate material of a same conductivity type of said monocrystalline substrate."

Tsu relates to "an integrated circuit capacitor and a method of forming a capacitor." (Col. 1, lines 14-15). Tsu discloses that a capacitor may be used in a DRAM array, and that the memory array may be "embedded in a larger integrated circuit device." (Col. 7, lines 54-62; Col. 8, lines 61-67).

The subject matter of claims 62-64 and 67-71 would not have been obvious over Yamamoto, Bai and Tsu. Again, the Office Action fails to establish a *prima facie* case of obviousness. None of Yamamoto, Bai and Tsu, considered alone or in combination, discloses, teaches or suggests all limitations of amended independent claim 62. Yamamoto, Bai and Tsu fail to teach or suggest a "processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a monocrystalline substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein," as amended independent claim 62 recites.

Yamamoto, Bai and Tsu also fail to teach or suggest a buried conductive structure within a monocrystalline substrate, the conductive structure "forming at least a part of an interconnect between devices" and "being completely surrounded by monocrystalline material," as in the claimed invention.

In addition, a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Tsu. As noted above, the crux of Yamamoto is a method of burying layers within a substrate to "prevent an increase in the number of wiring layers formed on a substrate." (Abstract). Yamamoto teaches "implanting an impurity in a semiconductor substrate . . . to form an impurity-implanted layer in the semiconductor substrate, forming a contact hole extending from a surface of the semiconductor substrate and reaching the impurity-implanted layer, selectively etching the impurity-implanted layer to form a tunnel in the semiconductor substrate, and burying a conductive film in the tunnel and the contact hole." (Col. 6, lines 53-62). On the other hand, Tsu teaches a "low resistance and low capacitance contact to subsurface electrodes . . . achieved by using highly conductive subsurface connectors which may be isolated by low dielectric insulator" to form "[s]tacks of devices are formed simultaneously within bulk single crystal semiconductor." (Abstract). Thus, again, the only structure which Yamamoto and Tsu have in common is their substrate on which their respective elements are formed. Accordingly, the disclosure of Tsu cannot supplement the inadequacies of Yamamoto, and withdrawal of the rejection of claims 62-64 and 67-71 is respectfully requested.

Claims 65, 74 and 80 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of various cited prior art references, including Bai, Sato and Tsu. Applicants note that, as described above, the cited prior art references, whether considered alone or in combination, fail to teach or suggest all

limitations of independent 62, 72 and 76. Accordingly, withdrawal of the rejection of claims 65, 74 and 80 is also respectfully requested.

Allowance of the application is solicited.

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Respectfully submitted,

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